

SEMICONDUCTOR DEVICE, SEMICONDUCTOR PACKAGE FOR USE THEREIN,
AND MANUFACTURING METHOD THEREOF

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a small size semiconductor package, and more particularly, to a semiconductor package of substantially the same size ^{as} a semiconductor ^{chip} device referred to as a chip size package, a semiconductor device using the semiconductor device, and a manufacturing method of the semiconductor device.

2. Description of the Related Art

These days, various apparatus including semiconductor devices, particularly portable apparatus and movable apparatus are being miniaturized and lightened. Semiconductor devices for use in these apparatus are thus desired to be miniaturized and lightened accordingly.

In order to meet the demands, a package of substantially the same ^{size as} ~~size~~ of a semiconductor ^{chip} ~~device~~ referred to as a chip size package (hereinafter referred to as CSP) has recently been proposed, and some semiconductor devices using such a chip size package are implemented as products.

As a semiconductor device formed with a semiconductor

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element mounted on a CSP, for example, as shown in Fig. 8, one in which a semiconductor ^{chip} element 3 is mounted and fixed via bumps 2 on a semiconductor package 1 is known. In this semiconductor device, the semiconductor package 1 comprises a substrate 4, a conductive connecting pattern 5 formed on one side of the substrate 4, a conductive connecting pattern 6 formed on the other side of the substrate 4, and a wiring material 7 formed so as to pierce the substrate 4 for the purpose of making the connecting pattern 5 electrically connected to the connecting pattern 6. As the material of the substrate 4, ceramics are mainly used for the purpose of making smaller the difference of the coefficient of thermal expansion between the semiconductor ^{chip} element 3 and the substrate 4 and thus making smaller the thermal stress to be applied to the bumps 2 and the semiconductor element 3.

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The semiconductor ^{chip} element 3 is fixed to the substrate 4 of the semiconductor package 1 thus structured with the conductive connecting pattern 5 formed on the one side of the substrate 4 being electrically connected thereto via the bumps 2 provided on a surface 3a where the element is formed. External connecting terminals 8 such as solder balls for bonding the conductive connecting pattern 6 to a mother board (not shown) are

fixed to the conductive connecting pattern 6 formed on the other side of the substrate 4. By this, the bumps 2 of the semiconductor ^{chip} element 3 are electrically connected to the external connecting terminals 8 via the connecting pattern 5, the wiring material 7, and the connecting pattern 6.

The semiconductor ^{chip} element 3 thus mounted on the semiconductor package 1 is integrally fixed to the semiconductor package 1 by sealing the whole periphery of the junction between the substrate and the semiconductor ^{chip} element 3 with resin 9 referred to as underfile. It is to be noted that the resin 9 referred to as underfile also performs a function to disperse the above-mentioned thermal stress due to the difference of the coefficient of thermal expansion between the substrate 4 and the semiconductor ^{chip} element 3.

Fig. 9 illustrates another example of a semiconductor device formed with a semiconductor element mounted on a CSP. In Fig. 9, a semiconductor device 10 is generally referred to as a chip on board (COP). The semiconductor device 10 is formed by mounting and fixing a semiconductor ^{chip} element 13 via adhesive 12 or the like on a semiconductor package 11.

The semiconductor package 11 comprises a substrate 14 the material of which is glass epoxy resin or the like, a conductive

connecting pattern 15 formed on one side of the substrate 14, a conductive connecting pattern 16 formed on the other side of the substrate 14, and a wiring material 17 formed so as to pierce the substrate 14 for the purpose of making the connecting pattern 15 electrically connected to the connecting pattern 16.

A surface opposite to a surface 13a where the element is formed of the semiconductor ^{chip}~~element~~ 13 is fixed with the adhesive 12 to one side of the substrate 14 of the semiconductor package 11 thus structured. Further, an electrode (not shown) formed on the surface 13a where the element is formed of the semiconductor ^{chip}~~element~~ 13 is electrically connected to the connecting pattern 15 of the semiconductor package 11 via wires 18. External connecting terminals 19 such as solder balls for bonding the conductive connecting pattern 16 to a mother board (not shown) are fixed to the conductive connecting pattern 16 formed on the other side of the substrate 14. By this, the electrodes of the semiconductor ^{chip}~~element~~ 13 are electrically connected to the external connecting terminals 19 via the connecting pattern 15, the wiring material 17, and the connecting pattern 16. The semiconductor package 11 with the semiconductor ^{chip}~~element~~ 13 thus mounted thereon is further provided with resin 20 covering the one side of the substrate 14 and the semiconductor ^{chip}~~element~~ 13 for

the purpose of protecting the surface 13a where the element is formed and the wires 18. By this, the semiconductor ^{chip}~~element~~ 13 and the wires 18 are sealed with the resin 20.

However, with the semiconductor device shown in Fig. 8, in order to decrease the thermal stress between the substrate 4 and the semiconductor ^{Chip}~~element~~ 3, ceramics, which are expensive, have to be used as the material of the substrate 4, leading to high cost as a whole, which is a problem to be solved.

Further, with the semiconductor device 10 shown in Fig. 9, although, since the thermal stress between the substrate 14 and the semiconductor element 13 can be absorbed by the wires 18, glass epoxy resin, which is inexpensive, can be used as the material of the substrate 14, since the wires 18 are disposed so as to go around to the outer peripheral side of the semiconductor element 13 in this structure, the size of the semiconductor device 10 as a whole with respect to the semiconductor element 13 is large, and thus, the semiconductor device 10 can not sufficiently meet the demands for miniaturizing and thinning the semiconductor device.

SUMMARY OF THE INVENTION

The present invention is made in view of the above, and therefore an object of the invention is to provide a

semiconductor device which is of substantially the same size of
a semiconductor ^{chip} element, which thus sufficiently ^{meets} meeting the

a ^{chip} element thereon to fix the side of a surface where the element
a is formed of the semiconductor ^{chip} ~~element~~ to one side thereof, and
a connecting pattern provided on the other side of the substrate
a for electrical connection to the semiconductor ^{chip} ~~element~~, the
a substrate being provided with a ^{elongate opening} ~~through hole~~ formed from the one
side to the other side of the substrate.

side to the other side of the substrate.

a With this semiconductor package, since a ~~through hole~~ *elongate opening* is formed in the substrate and the connecting pattern is provided on the side of the substrate opposite to the side on which the surface where the ~~element~~ *chip* is formed of the semiconductor element is mounted, an electrode formed on the surface where the element is formed of the semiconductor ~~element~~ *chip* and the connecting pattern can be bonded with wires through the ~~through hole~~ *elongate opening*. Accordingly,

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the semiconductor ^{chip}~~element~~ and the connecting pattern of the substrate are bonded with wires through the ^{elongate opening}~~through hole~~, the wires can be disposed without going around to the outer peripheral side of the semiconductor ^{chip}~~element~~. This eliminates the necessity of space for the wires on the outer peripheral side of the semiconductor ^{chip}~~element~~.

Further, since the semiconductor ^{chip} element and the substrate are bonded with the wires, the wires can absorb the difference of the coefficient of thermal expansion between the semiconductor ^{chip} element and the substrate, which makes it possible

the steps of preparing a semiconductor package structured by
 a providing a substrate for mounting a semiconductor ^{chip} element
 thereon to fix the semiconductor ^{chip} element to one side thereof and

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to be noted that the semiconductor package 31 in the semiconductor device 30 is a first embodiment of a semiconductor package according to the first aspect of the present invention.

In the semiconductor device 30, the semiconductor package

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31 comprises a rectangular substrate 33 for mounting the semiconductor ^{chip} ~~element~~ 32 thereon to fix the side of a surface 32a where the element is formed of the semiconductor ^{chip} ~~element~~ 32 to one side thereof, and a plurality of connecting patterns 34

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provided on the other side of the substrate 33. The material of the substrate 33 is glass epoxy, resin or the like. As shown in Fig. 2A, a ^{elongate opening} ~~through hole~~ 35 is formed along the longitudinal center line of the substrate 33. The ^{elongate opening} ~~through hole~~ 35 is formed

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as a rectangular opening from the one side to which the semiconductor ^{chip} ~~element~~ 32 is fixed to the other side. It is to be noted that, as shown in Figs. 1 and 2A, the respective connecting patterns 34 are formed so as to extend from

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longitudinal edge portions of the substrate 33 to the ^{elongate} ~~through~~ ^{opening} ~~hole~~ 35, and are made of metal or the like and are conductive.

As shown in Figs. 1 and 2B, an insulating film 36 covering the connecting patterns 34 with the connecting patterns 34 being partly exposed is formed on the other side of the substrate 33 on which the connecting patterns 34 are formed. The insulating film 36 is made of resist or the like, and is provided with end portions 34a of the connecting patterns 34 on the side of the ^{elongate opening} ~~through hole~~ 35 and portions other than the end portions 34a, in this example, end portions 34b opposite to the end

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portions 34a, exposed, and with the through hall 35 left opened,
i.e., without covering the ~~through hall 35~~ *elongate opening*.

As shown in Figs. 1 and 2C, a tape-like bonding material 37 is provided on the one side of the substrate 33 of the semiconductor package 31 thus structured with a portion around the longitudinal center line of the ~~through hole~~ *elongate opening* 35 being opened. The bonding material 37 is formed by applying thermoplastic adhesive such as polyamideimide or thermosetting adhesive such as modified epoxy resin on both sides of a tape base material made of resin such as polyimide.

As shown in Fig. 1, the semiconductor ~~element~~ ^{chip} 32 is mounted and fixed via the bonding material 37 on the one side of the substrate 33. As shown in Fig. 3, the semiconductor ~~element~~ ^{chip} 32 is like a rectangular plate with a plurality of electrodes 38 formed on the longitudinal center line of the surface 32a where the element is formed. The electrodes 38 are disposed within the

As shown in Figs. 1 and 4, the electrodes 38 of the semiconductor element 32 disposed within the through hall 35 are connected to the end portions 34a of the connecting patterns 34 via wires 39 through the ~~through hall~~ ^{chip} 35. By this, the electrodes 38 are electrically connected to the connecting

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elongate opening
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with the insulating resin 41 such as epoxy resin, and the insulating resin 41 is applied so as to cover the wires 38 and the end portions 34a of the connecting patterns 34 to seal all of the electrodes 38, the wires 39, and the end portions 34a of the connecting patterns 34.

After that, the external connecting terminals 40 such as solder balls are bonded to the respective end portions 34b of the connecting patterns 34 under high temperature to obtain the semiconductor device 30.

With the semiconductor device 30 thus obtained, since the electrodes 38 formed on the surface 32a where the element is formed of the semiconductor ^{chip}element 32 and the connecting patterns 34 of the substrate 33 are bonded with the wires 39 through the ^{elongate opening}~~through hole~~ 35, it is not necessary to provide space for the wires 39 on the outer peripheral side of the semiconductor ^{chip}element 32, which leads to miniaturizing and thinning the device as a whole.

Further, since the semiconductor ^{chip}element 32 and the substrate 33 are bonded with the wires, the wires 39 can absorb the difference of the coefficient of thermal expansion between the semiconductor ^{chip}element 32 and the substrate 33, which makes it possible to use an inexpensive resin substrate instead of an

expensive ceramics substrate.

Fig. 6 illustrates a second embodiment of a semiconductor device according to the fourth aspect of the present invention. The difference between a semiconductor device 50 in Fig. 6 and the semiconductor device 30 shown in Fig. 1 resides in the structure of a semiconductor package 51 in the semiconductor device 50. The semiconductor package 51 in the semiconductor device 50 is a second embodiment of a semiconductor package according to the first aspect of the present invention. The semiconductor package 51 differs from the semiconductor package 31 shown in Fig. 1 in that its connecting patterns 52 are formed in a plurality of stages (two stages in this example).

More specifically, a substrate 53 of the semiconductor package 51 is formed of an upper plate 53a and a lower plate 53b. The lower plate 53b is formed such that its edge on the side of a ~~through hole~~ *elongate opening* 54 is outside an edge of the upper plate 53a. By this structure, the rear surface (the other side) of the substrate 53 is formed to be in two stages, i.e., the rear surface of the upper plate 53a and the rear surface of the lower plate 53b.

A first plurality of connecting patterns 52a are provided on the rear surface of the upper plate 53a of the substrate 53.

A second plurality of connecting patterns 52b are provided on the rear surface of the lower plate 53b. The first and the second connecting patterns 52a and 52b are electrically connected to each other via a wiring material 55 provided so as to pierce the lower plate 53b. By this structure, the connecting patterns 52 are in two stages (a plurality of stages) formed by the first connecting patterns 52a, the wiring material 55, and the second connecting patterns 52b.

An insulating film 56 is formed on the rear surface of the lower plate 53b so as to cover the second connecting patterns 52b. It is to be noted that, in this example also, the insulating film 56 is formed with the second connecting patterns 52b being partly exposed, that is, similarly to the one shown in Fig. 2B, with longitudinal end portions of the substrate 53 being exposed.

In the ~~through hole~~ ^{elongate opening} 54 formed with the stages in the substrate 53 formed of the upper plate 53a and the lower plate 53b in this way, the electrodes 38 of the semiconductor ^{chip} element 32 disposed within the ~~through hole~~ ^{elongate opening} 54 are connected via the wires 39 to the end portions of the first connecting patterns 52a exposed on the rear surface of the upper plate 53a of the substrate 53. Further, the ~~through hole~~ ^{elongate opening} 54 is filled with

insulating resin 57 covering the wires 39 and the end portions of the first connecting patterns 52a. By this, the electrodes 38, the wires 39, and the end portions of the first connecting patterns 52a are sealed and insulated from the external.

With the semiconductor device 50 thus structured, similarly to the case of the semiconductor device 30 shown in Fig. 1, since it is not necessary to provide space for the wires 39 on the outer peripheral side of the semiconductor ^{chip} element 32, the device can be miniaturized and thinned as a whole. Further, since the wires 39 can absorb the difference of the coefficient of thermal expansion between the semiconductor ^{chip} element 32 and the substrate 53, an inexpensive resin substrate can be used as the substrate 53.

Still further, since the substrate 53 is formed in two stages of the upper plate 53a and the lower plate 53b, and the connecting patterns 52 are in two stages (a plurality of stages) formed by the first connecting patterns 52a, the wiring material 55, and the second connecting patterns 52b, such that the wires 39 are connected to the end portions to the central side of the substrate 53, that is, to the end portions provided on a stage on the side of the one side of the substrate 53, the wires 39 may be cased within the ^{elongate opening} ~~through hole~~ 54 without extending to the

outside. By this, the wires 39 can be covered with the insulating resin 57 just by filling the ~~through hall~~ *elongate opening* 54 with the insulating resin 57 at the bottom of the substrate 53 without heaping up the insulating resin 57 on the rear surface of the lower plate 53b. Accordingly, the diameter of the external connecting terminals 40 such as solder balls can be made small, which leads to finer pitch of the external connecting terminals 40.

Fig. 7 illustrates a third embodiment of a semiconductor device according to the fourth aspect of the present invention. The difference between a semiconductor device 60 in Fig. 7 and the semiconductor device 30 shown in Fig. 1 resides in the structure of a semiconductor package 61 in the semiconductor device 60. The semiconductor package 61 in the semiconductor device 60 is a third embodiment of a semiconductor package according to the first aspect of the present invention. The semiconductor package 61 differs from the semiconductor package 31 shown in Fig. 1 mainly in that a plurality of ~~through halls~~ *elongate opening* 63, two through halls 63 in this example, are formed in a substrate 62.

More specifically, two lines of the ~~through halls~~ *elongate openings* 63 are formed in the substrate 62 of the semiconductor package 61 along

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a formed on the surface where the element is formed of the
 a semiconductor ^{chip}~~element~~ and the connecting pattern of the substrate
 are bonded with wires through the ^{elongate opening}~~through hole~~, the wires can be
 disposed without going around to the outer peripheral side of the
 a semiconductor ^{chip}~~element~~. This eliminates the necessity of space
 for the wires on the outer peripheral side of the semiconductor
 a ^{chip}~~element~~, and thus, the device can be miniaturized and thinned as
 a whole.

a Further, since the semiconductor ^{chip}~~element~~ and the
 substrate are bonded with the wires, the wires can absorb the
 difference of the coefficient of thermal expansion between the
 a semiconductor ^{chip}~~element~~ and the substrate, which makes it possible
 to use an inexpensive resin substrate instead of an expensive
 ceramics substrate. By this, the cost of the semiconductor
 device can be lowered.

a In the method of manufacturing a semiconductor device
 according to the seventh aspect of the invention, since the
 semiconductor package of the first aspect of the present
 invention is used, and the electrode formed on the surface where
 the element is formed of the semiconductor ^{chip}~~element~~ and the
 connecting pattern of the substrate are bonded with wires through
 a ^{elongate opening}~~through hole~~, the wires can be disposed without going around

a to the outer peripheral side of the semiconductor ^{chip}~~element~~. This eliminates the necessity of space for the wires on the outer peripheral side of the semiconductor ^{chip}~~element~~, and thus, the device can be miniaturized and thinned as a whole.

a Further, since the semiconductor ^{chip}~~element~~ and the substrate are bonded with the wires, the wires can absorb the difference of the coefficient of thermal expansion between the semiconductor ^{chip}~~element~~ and the substrate, which makes it possible to use an inexpensive resin substrate instead of an expensive ceramics substrate. By this, the cost of the semiconductor device can be lowered.

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